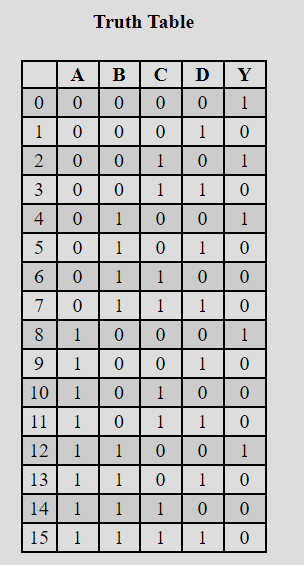
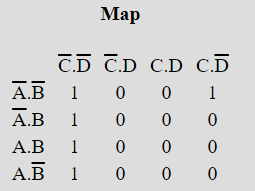
|  |  |
| --- | --- |
| **Digital Circuits** | **Year 2020** |
| **Laboratory report** | **Number of the exercise: 2** |
|  |  |
| 1. Name and surname (author of realized | **Title of the exercise: Combinational Logic Circuits** |
| circuit/this report): Nykonchuk Illia |  |
| CAD1 |  |
|  |  |
|  |  |
|  |  |
| Laboratory group number: | Week day: Thursday |
|  | Realization date:27.03.2020 |
| Breadboard number: | Hours of the lab:17:05-18:45 |
|  |  |

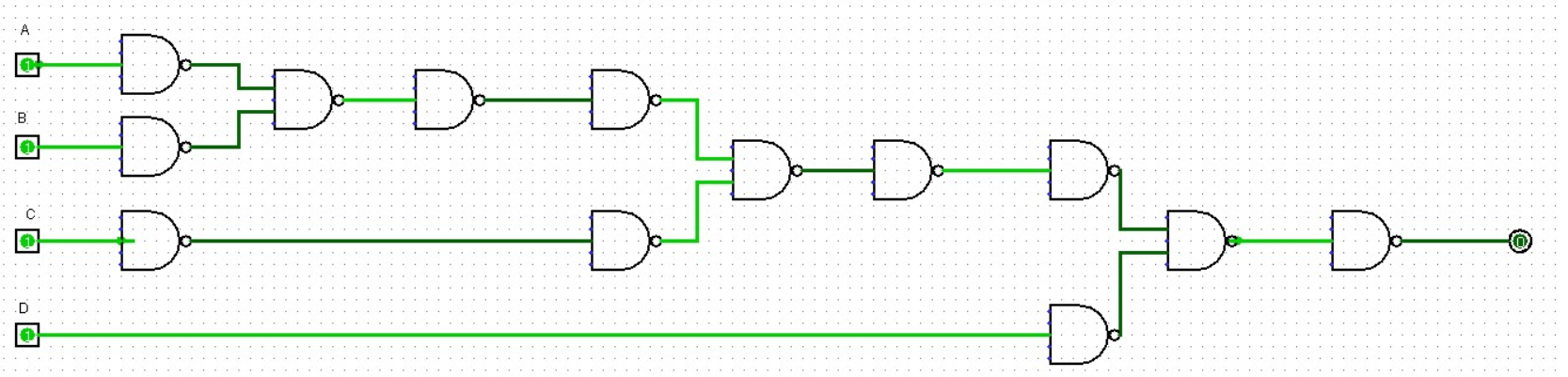
Functions



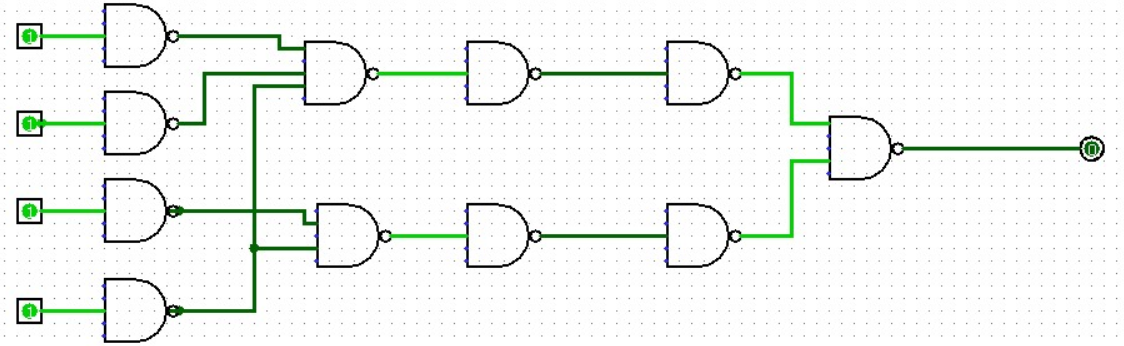
Truth table and Karnaugh Map:

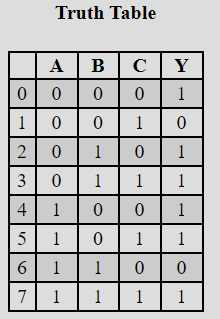


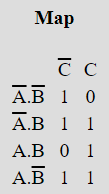
Circuit by using only NAND gates:



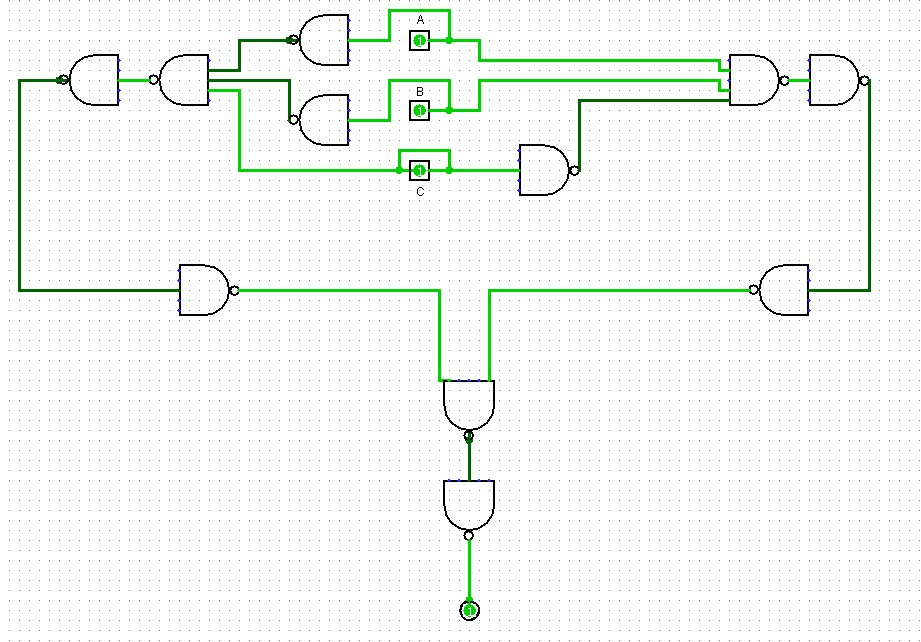
And it’s minimized version using Karnaugh map:



Truth table and Karnaugh map:



Circuit by using only NAND gates:



And it’s minimized version using Karnaugh map:

